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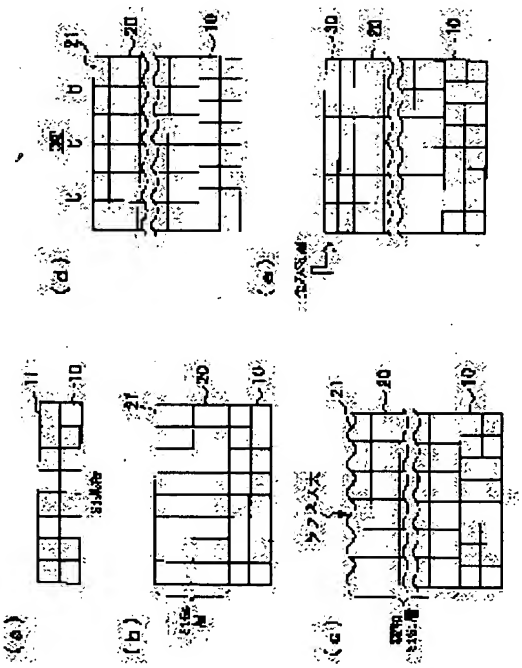
(54) METHOD FOR POLISHING SURFACE OF SEMICONDUCTOR, METHOD FOR FABRICATING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for polishing the surface of a semiconductor in which surface roughness can be reduced while suppressing through dislocation, a method for fabricating a semiconductor device and a semiconductor device.

SOLUTION: On the surface 11 of an Si substrate 10, an SiGe layer 20 having a lattice constant different from that of the Si substrate 10 is grown. The SiGe layer 20 is formed by graded composition buffer method until it has a sufficient thickness and then growth is relaxed. Subsequently, the surface of the SiGe layer 20 is polished by CMP where roughness on the surface 21 of the SiGe layer 20 can be decreased as low as several nm in RMS value. Since Si is grown on a planarized surface 21, a strained Si layer 30 having high planarity can be obtained. In the strained Si layer 30, through dislocation is suppressed and surface roughness is reduced.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the polish approach on the front face of a semiconductor, the manufacture approach of a semiconductor device, and a semiconductor device.
[0002]
[Background of the Invention] With the detailed-ized technique which progresses every year, ULSI became the high integration and accelerable and has contributed to implementation of today's highly informative society. In ULSI, since many Si-MOSFET (Metal Oxide Semiconductor Field Effect Transistor, MOS electric field effect mold transistor) produced on (Silicon Si) substrate is used, research towards detailed-ization of Si-MOSFET has been done briskly. However, it is inevitable that a limitation visits to the detailed-ization from now on, and the research which raises the mobility of the electron which is bearing actuation of MOSFET is progressing towards the further improvement in the speed. In MOSFET using GaAs, such an attempt is already made by the ingredient and MOSFET which an electron can move [high-speed] is put in practical use. However, Si exists on the earth rather than Ga or As at abundance, is cheap and, moreover, has the outstanding description that no damage done to the body or an environment is. Therefore, the usefulness is large if high-speed MOSFET is producible on Si substrate.
[0003] Then, the method of using as follows SiGe which is the mixed crystal which mixed germanium (germanium) with Si was invented. If Si is made to deposit on SiGe with the larger interatomic distance (lattice constant) than Si (growth), Si layer (distortion Si layer) from which the interatomic distance differs in a direction and the growth (length) direction in a field (width) is produced, and it turns out that mobility goes up the electron in it. Then, implementation of distortion Si-MOSFET which uses this distortion Si layer as the channel (path as an electron) of MOSFET is expected. In addition, high-speed operation is expected and MOSFET which uses distortion SiGe and distortion germanium as a channel is also studied.
[0004] In order to produce the high speed MOSFET which introduced these distortion on Si substrate, it is required to be common in all and to grow up a "strain relaxation SiGe buffer layer" on Si substrate. The method of producing distortion Si is typically shown in drawing 7 . If SiGe is made to deposit gradually on the crystal Si substrate 1 shown in this drawing (a) (this drawing b), it will grow up with the same lattice constant as Si in the beginning. It is made to grow up furthermore, and if thickness with the SiGe layer 2 is exceeded, it will return to the original lattice constant of SiGe (this is called relaxation.). Refer to drawing 5 c. Then, on the eased SiGe layer (there is only a "strain relaxation SiGe buffer layer" or a "buffer layer" below.) 2, Si is grown up, it deposits and the Si layer 3 is formed. Since this Si layer 3 grows with the same lattice constant as SiGe, it turns into a distortion Si layer. If MOSFET is produced using this distortion Si layer 3, distortion Si-MOSFET will be completed. By this approach, in order for the process itself which produces MOSFET not to be different from the case of MOSFET on mere Si substrate at all, it has the advantage that this production is easy.
[0005] Thus, in order to realize a SiGe system high-speed device like distortion Si-MOSFET which

introduced distortion into the channel, the good strain relaxation SiGe layer buffer layer 2 is required. However, since the penetration rearrangement to which the front face of the buffer layer 2 extends even in the increase of roughness (irregularity) and a channel exists in high density in connection with strain relaxation, the mobility of the electron in a channel will fall remarkably. Then, various methods of producing a strain relaxation SiGe buffer layer are tried. But a general approach is the inclination presentation buffer method for raising germanium concentration of a SiGe layer gradually. However, if a penetration rearrangement is stopped, surface roughness will become large, there is an inclination for penetration dislocation density to go up if it is going to make a front face flat, and the buffer grown method which can reduce both surface roughness and penetration dislocation density does not yet exist. Although there is the other low-temperature buffer method for the ability to stop surface roughness sharply, this also has the problem that penetration dislocation density is large.

[0006]

[Problem(s) to be Solved by the Invention] This invention was made in view of the aforementioned situation, and the purpose is offering the polish approach on the front face of a semi-conductor which can make surface roughness small, the manufacture approach of a semiconductor device, and a semiconductor device, stopping a penetration rearrangement.

[0007]

[Means for Solving the Problem] Corresponding to this technical problem, the polish approach on the front face of a semi-conductor according to claim 1 has the following step.

(a) the step which grows up into the front face of the 1st semi-conductor this 1st semi-conductor and the 2nd semi-conductor with which lattice constants differ, and (b) -- the step which makes said 2nd semi-conductor ease, and (c) -- the step which grinds the front face of said 2nd semi-conductor by the CMP method.

[0008] The polish approach on the front face of a semi-conductor according to claim 2 shall consist the 1st semi-conductor of Si in a thing according to claim 1.

[0009] The polish approach on the front face of a semi-conductor according to claim 3 shall consist the 2nd semi-conductor of SiGe in a thing according to claim 1 or 2.

[0010] In the thing according to claim 1 to 3, it was presupposed to the polish approach on the front face of a semi-conductor according to claim 4 that the 2nd semi-conductor is formed by the inclination presentation buffer method. Here, the inclination presentation buffer method means the crystal growth method which is made to carry out the change rise of the ratio of the accessory constituent to a principal component gradually, and goes.

[0011] The polish approach on the front face of a semi-conductor according to claim 5 is a thing given in any 1 term of claims 1-4, and the 5000A or more laminating of said 2nd semi-conductor is carried out to the front face of said 1st semi-conductor in the step (a).

[0012] The manufacture approach of a semiconductor device according to claim 6 manufactures a semiconductor device by growing up the 3rd semi-conductor into the front face of said 2nd semi-conductor ground by the polish approach on the front face of a semi-conductor in any 1 term of claims 1-5.

[0013] A semiconductor device according to claim 7 is a semiconductor device which comes to carry out the laminating of the 3rd semi-conductor which has distortion on the front face of the 2nd semi-conductor, and the roughness of the front face of said 2nd semi-conductor has been less than [RMS=10nm].

[0014] In the thing according to claim 7, the roughness of the front face of said 2nd semi-conductor of the semiconductor device according to claim 8 has been less than [RMS=1nm].

[0015] In the thing according to claim 7 or 8, the thickness of said 2nd semi-conductor of the semiconductor device according to claim 9 has been 500A - 1 micrometer.

[0016] In the thing according to claim 9, the thickness of said 2nd semi-conductor of the semiconductor device according to claim 10 has been 1000A or more.

[0017] In the thing according to claim 9 or 10, the thickness of said 2nd semi-conductor of the semiconductor device according to claim 11 has been 5000A or less.

[0018] The manufacture approach of a semiconductor device according to claim 12 has the composition of manufacturing a semiconductor device using the 2nd semi-conductor ground by the polish approach on the front face of a semi-conductor in any 1 term of claims 1-5.
[0019] The semiconductor device according to claim 13 has composition manufactured by the manufacture approach of a semiconductor device according to claim 6 or 12.
[0020]
[Function] If flattening of the large buffer layer front face of roughness can be carried out by polish, both penetration dislocation density and surface roughness can obtain a low strain relaxation SiGe buffer layer. It is the sample produced by the inclination presentation buffer method Chemical Mechanical Polishing Flattening of the front face can be carried out by grinding with a technique (CMP).
[0021]
[Embodiment of the Invention] The polish approach on the front face of a semi-conductor concerning 1 operation gestalt of this invention, the manufacture approach of a semiconductor device, and a semiconductor device are explained below. First, the polish approach is explained based on drawing 1 .
[0022] First, the SiGe layer (the 2nd semi-conductor) 20 which is the semi-conductor with which this Si substrate 10 and lattice constant differ from each other on the front face 11 of the Si substrate (the 1st semi-conductor) 10 shown in drawing 1 (a) is grown up (drawing 1 b). as this growth approach -- a CVD method and the gas source MBE -- the thing of arbitration, such as law, can be used. Since the growth approach itself is the same as usual, explanation of a detail is omitted. Here, although Si was used as a presentation of the 1st semi-conductor with this operation gestalt, otherwise, it is possible to use germanium. Moreover, the SiGe layer 20 is formed by the inclination presentation buffer method here. Make initiation germanium concentration into 0%, and germanium concentration is made to specifically increase by the fixed multiplier, and it controls and forms so that termination (upper limit) germanium concentration may be made into the purpose concentration (30% of for example, germanium concentration). From the former, since such a formation approach is well-known, it omits explanation of a detail.
[0023] Subsequently, the SiGe layer 20 is grown up until it becomes sufficiently thick, and the SiGe layer 20 is made to ease. As for the thickness of the SiGe layer 20, with this operation gestalt, considering as 5000A or more is desirable. Thereby, the SiGe layer 20 becomes an original lattice constant. Then, irregularity arises in the front face 21, and roughness becomes large on it (drawing 1 c). In addition, it does not pass over the irregularity shown in drawing 1 to what was shown notionally, but, as for the period, it is general that it is larger than a lattice constant. It is the same as that of the conventional technique fundamentally so far.
[0024] Subsequently, the front face 21 of the SiGe layer 20 is ground by the CMP method (drawing 1 d). Although the thing which made the alkali solution of pH 11 [10.5-]11, for example, pH, distribute the mean particle diameter of 30nm - 80nm, for example, 70nm colloidal silica, can be used as a presentation of the slurry used for polish, it is not limited to this. The range of 500A - 1 micrometer of thickness of the SiGe layer 20 after polish is 1000A or more or 5000A or less further preferably. Since the CMP polish approach except said is the same as usual, explanation of a detail is omitted.
[0025] According to the approach of this operation gestalt, by this CMP polish, the roughness of the front face 21 of the SiGe layer 20 can be reduced in an RMS value to 10nm or less (the example of an experiment mentioned later 1nm or less) by spending a certain amount of polish time amount (for example, about 10 minutes). RMS is the standard deviation of measured value (equivalent to surface height), and can be obtained here by taking the sum about all point of measurement, dividing the square of (an average of measured-value-all measured value) by the number of the fixed points a side, and taking the square root of the **.
[0026] Thus, by growing up Si into the front face 21 by which flattening was carried out, the high distortion Si layer 30 of display flatness can be obtained. The growth approach of this distortion Si layer 30 itself is the same as usual. In the Prior art, since there was relation that the roughness of a front face 21 increases when penetration dislocation density tends to go up if flattening of the front face 21 of the SiGe layer 20 tends to be carried out, and it is going to lower penetration dislocation density, it was

difficult to lower the roughness of a front face 21 enough. On the other hand, according to the approach of this operation gestalt, the SiGe layer 20 can be grown up so that penetration dislocation density may become low, and the irregularity of the front face 21 produced as a result can be lowered to the RMS value equivalent to a number atomic layer by the CMP method. Therefore, there is an advantage that the front face 21 where penetration dislocation density has roughness low enough low can be obtained. Therefore, the Si layer 30 by which the laminating was carried out on this front face 21 will have high display flatness.

[0027] MOS-FET (semiconductor device) is producible by making the gate, the source, and a drain in the Si layer 30 formed as mentioned above. Since this production approach itself is the same as usual, explanation is omitted. Thus, since the display flatness of the Si layer 30 used as a channel is high according to constituted MOS-FET, there is an advantage that there is little dispersion of a carrier and it can raise the mobility. Then, even if it does not use GaAs, the high-speed semiconductor device by Si can be obtained, and the advantage is large also in respect of cost or safety. Furthermore, since it is realizable with the easy step in comparison, each approach of this operation gestalt also has the advantage that operation is easy.

[0028] In addition, although [said operation gestalt] a semiconductor device is produced using the distortion Si layer 30, it is also possible to consider as a semiconductor device by making a channel, the gate, and the source to SiGe layer 20 eased the very thing.

[0029]

[Example(s) of Experiment] (Experiment conditions) It experimented on the same experiment conditions as the above mentioned operation gestalt. Still more detailed conditions are shown below. (1) presentation [of the SiGe layer 20]: -- (4) during presentation (3) polish time amount:10 minutes polish thickness (polish thickness): to which initiation germanium concentration made the alkali solution of pH11 distribute the colloidal silica with a presentation:mean particle diameter of 70nm of the presentation (2) slurry from which termination (upper limit) germanium concentration becomes 30% (Remainder Si and unescapable impurity) 0% by the inclination presentation buffer method -- 100nm

[0030] It ground the above condition. The result is shown in drawing 2 R> 2. Among drawing, (a) shows the front face of the SiGe layer before polish, and (b) shows the front face after polish among drawing. Clearly, it turns out that display flatness is improving sharply.

[0031] In addition, according to this invention person's experimental result, the relation between polish thickness and surface roughness came to be shown in drawing 3 . This result shows that very high display flatness [say / RMS=0.5nm] can also be realized.

[0032] In addition, as for the polish front face after CMP, the abrasive material has adhered in large quantities, and if optimal washing is not performed, a good epitaxial film cannot re-grow on it. Then, this invention persons removed adhesion particle completely by washing which used the surface active agent. In order that washing might dip a polish front face in 1:1.ammonia:hydrogen-peroxide:water =5:70 70-degree C mixed solution for 10 minutes and might stop the reattachment of particle after that, it carried out the rinse with the ultrapure water which added the organic sulfonic acid 0.1%, and performed over flow rinse for 10 minutes with ultrapure water further. Next, it dipped in fluoric acid for 30 seconds 0.5% for oxide-film removal. In addition, in order to prevent the reattachment of the particle which remained in the inside of an oxide film, or a front face, the organic sulfonic acid was added also to fluoric acid 0.1%. Drawing 4 shows a washing result, this drawing (a) is before washing and this drawing (b) is a surface AFM image after washing. It turns out that particle is completely removed by washing.

[0033] In order to perform such washing after CMP and to remove metal contamination and organic substance contamination further, after performing sulfuric-acid hydrogen-peroxide-solution washing, SiGe was grown up again. Photoluminescence was observed from the quantum well which this constituted. Therefore, the good EPI film was able to be grown up on the polished surface. Moreover, it was checked that the front face of the SiGe film re-grown up is also the RMS value of 1nm or less. That is, it succeeded in obtaining a SiGe (it setting to upper limit and being germanium30%) buffer layer with display flatness which was not able to be produced until now and which is called the surface RMS

roughness value of 1nm or less.
[0034] Furthermore, as a result of investigating about the polishing pressure force and a polish rate, relation like drawing 5 was obtained. The polish rate was proportional to the polishing pressure force mostly, and it turned out that it is so quick that germanium concentration of SiGe is so large that the particle size of an abrasive material is large. Although it is necessary to change the suitable polishing pressure force into arbitration by germanium concentration of a sample, the roughness before polish, and the abrasive material, it is thought that 100 - 800 g/cm2 is suitable for it.
[0035] Furthermore, this invention person ground various samples and investigated the difference in the attainment display flatness by the sample (drawing 6 R> 6). Consequently, it is thought that it depends for attainment display flatness on the surface defect density (it is thought that it is proportional to the surface roughness after SEKOETCHI) of a buffer layer greatly. that is, the thing for which a buffer layer from which the roughness after SEKOETCHI performed after CMP is set to 5nm or less is produced in order to obtain the front face not more than RMS roughness 1nm -- it is thought that it is desirable. It is expected that the best polish corresponding to a crystal defect consistency is realizable by furthermore adjusting pH of an abrasive material.
[0036] In addition, the publication of said operation gestalt and an example is not what did not pass to a mere example but showed the indispensable configuration to this invention. The configuration of each part will not be restricted above, if the meaning of this invention can be attained.
[0037]
[Effect of the Invention] According to this invention, the polish approach on the front face of a semiconductor which can make surface roughness small, the manufacture approach of a semiconductor device, and a semiconductor device can be offered, stopping a penetration rearrangement.

[Translation done.]

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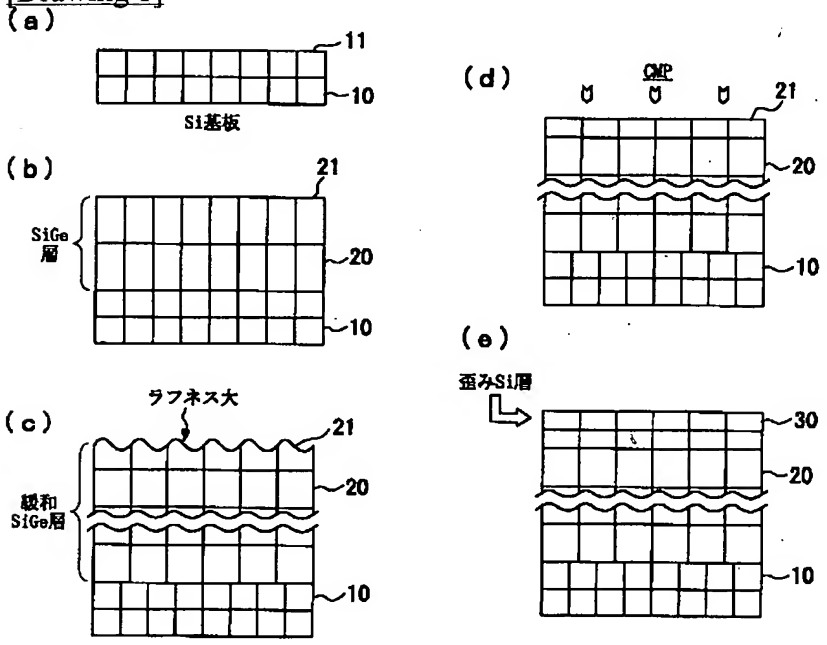
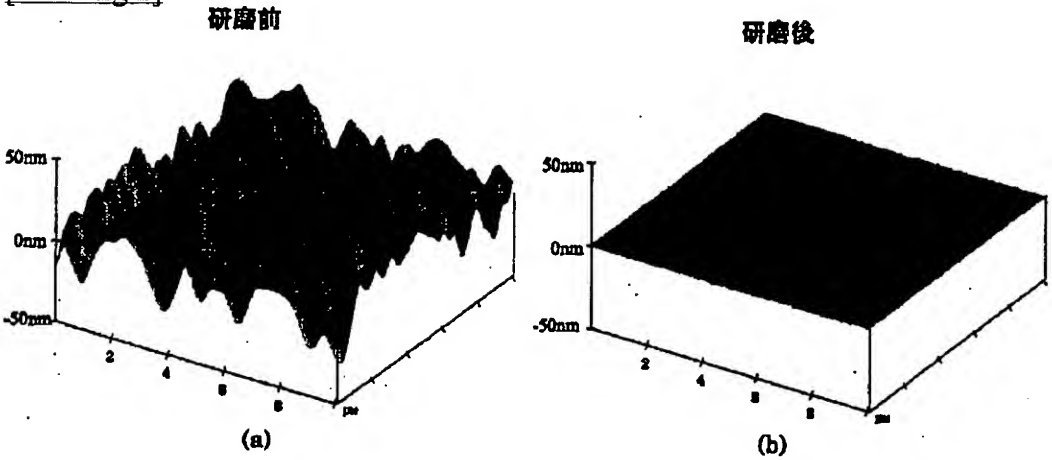
DRAWINGS

[Drawing 1]

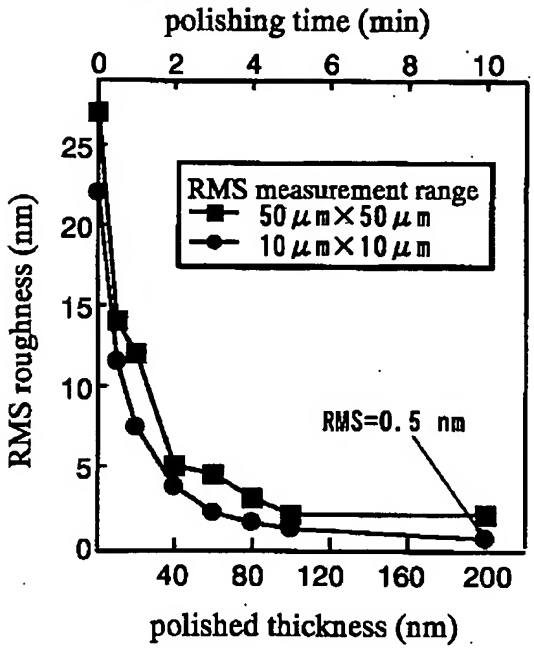


[Drawing 2]



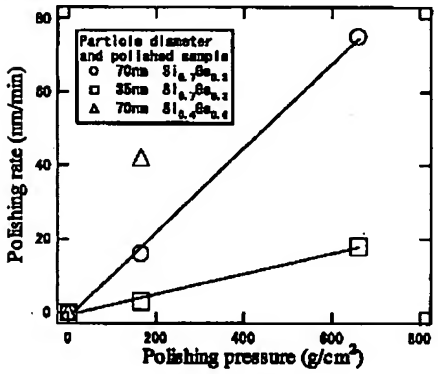
研磨前後の歪み緩和SiGeバッファー層表面のAFM像

[Drawing 3]



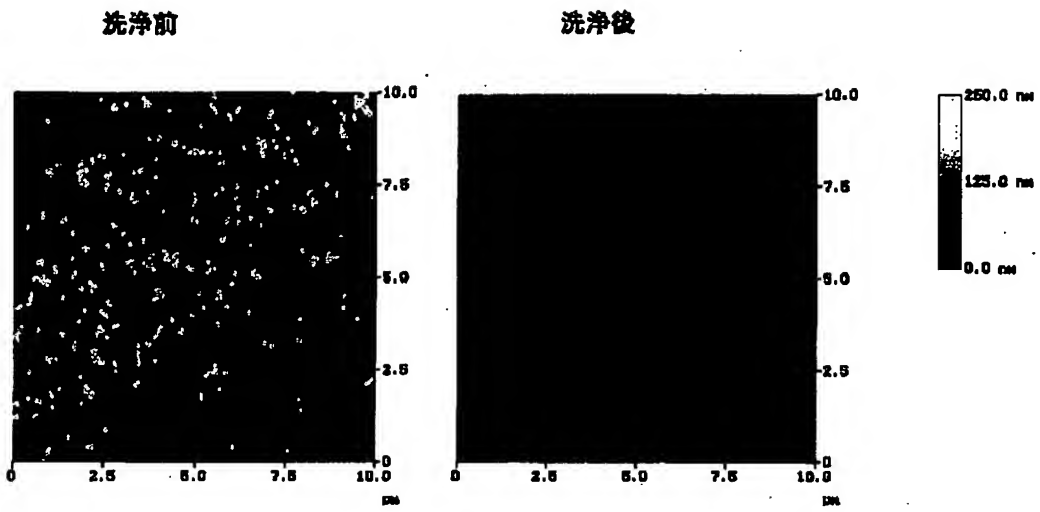
研磨膜厚（研磨時間）による RMS ラフネスの変化

[Drawing 5]



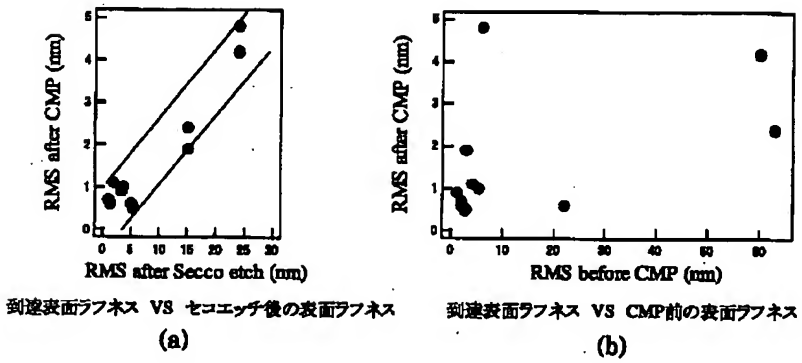
研磨速度と研磨圧力の関係

[Drawing 4]

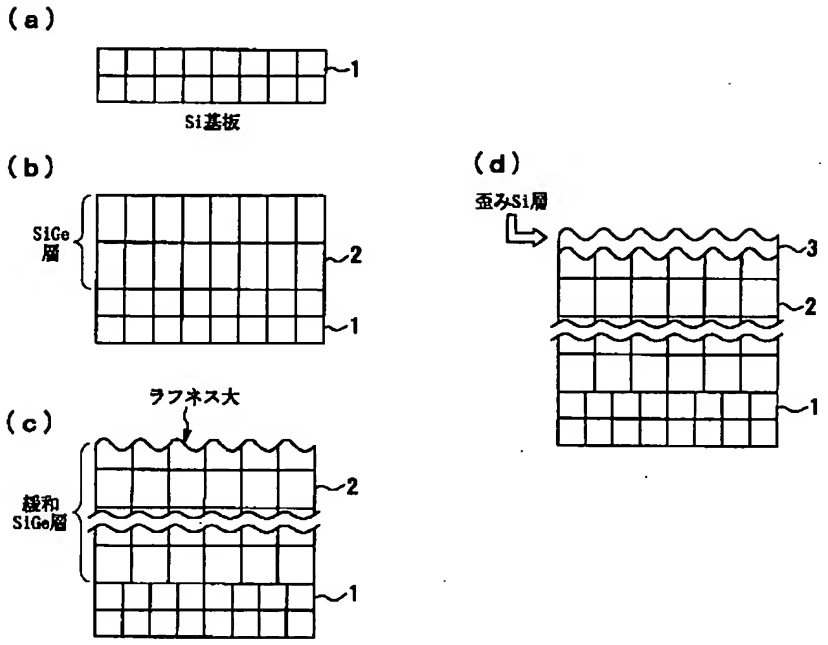


洗浄前後の表面AFM像

[Drawing 6]



[Drawing 7]



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